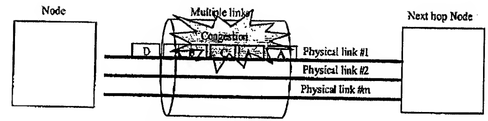
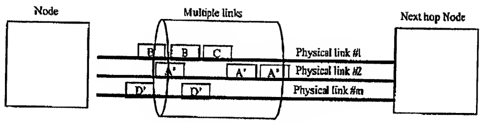
Fig.1



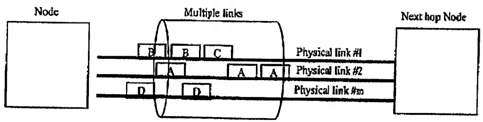
Without load balance mechanism

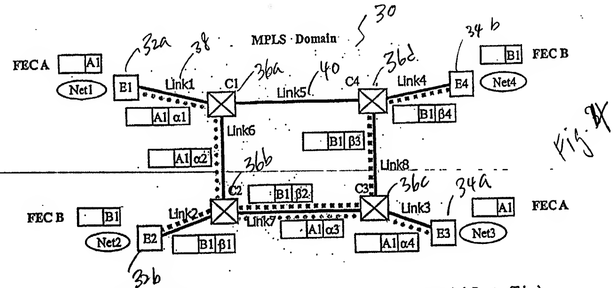
Fig.2



) With Conventional load balance mechanism

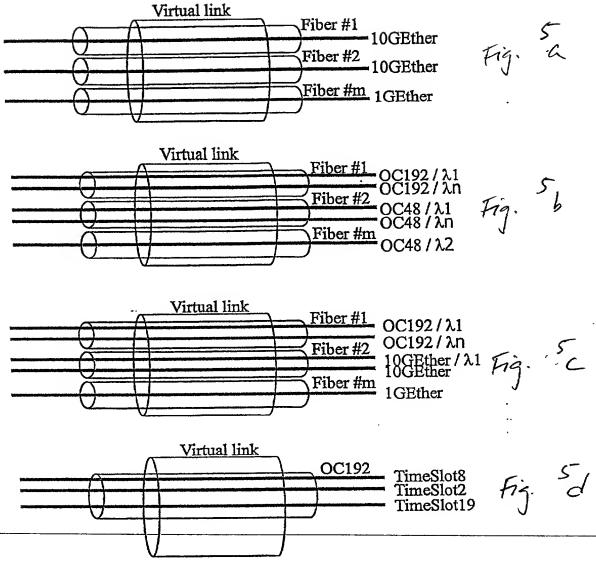
Fig.3





C1, C2, C3, C4 : Label Switch Router (CORE), E1, E2, E3, E4 : Label Switch Router (Edge),
A1, B1: IP Destination Address, α1, α2, α3, α4 , β1, β2, β3, β4 : Label

[redacted] Example of the network (MPLS) domain



Examples of composition of physical and logical links

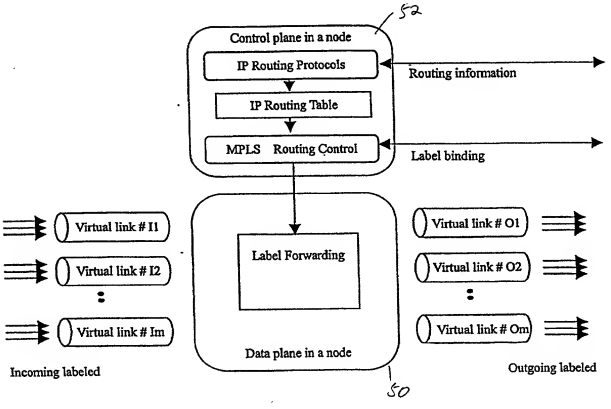


Figure 6 LSR Architecture

Figure 7

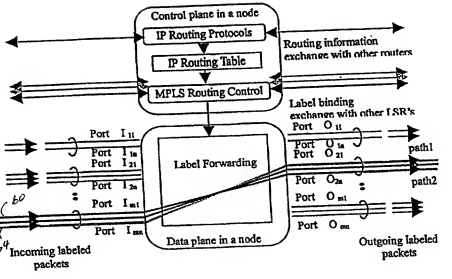
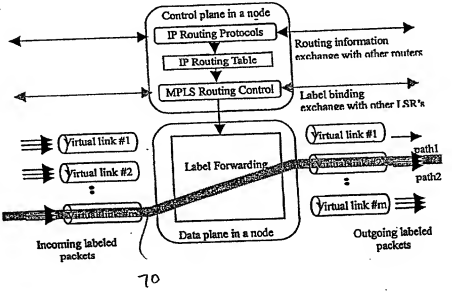
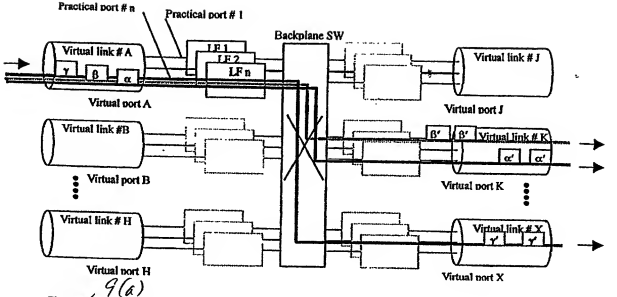


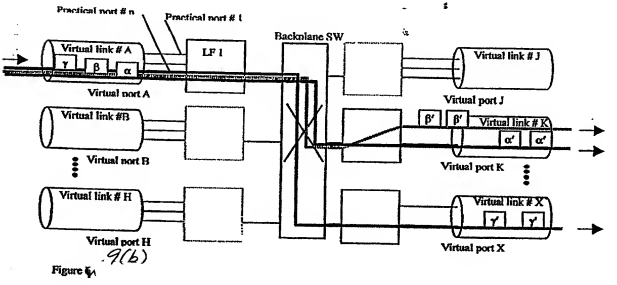
Figure 8





9(a)

Figure 9(a)



9(b)

Figure 9(b)

Label Forwarding Table maintained by the MPLS control plane

Input practical port #	Input virtual port #	Input Label	Output Label	Output virtual port #	Output practical port #
n	A	α	α'	K	$f(\alpha')$
n	A	β	β'	K	$f(\beta')$
n	A	γ	γ'	X	$f(\gamma')$
2	A	δ	δ'	B	$f(\delta')$
1	A	ε	ε'	B	$f(\varepsilon')$
2	A	ζ	ζ'	H	$f(\zeta')$
1	A	η	η'	J	$f(\eta')$
5	A	σ	σ'	K	$f(\sigma')$
n	A	κ	κ'	X	$f(\kappa')$

Figure 10 Label Forwarding Table and mechanism to decide practical output port at the sending LSR

Label Forwarding Table maintained by the MPLS control plane

Tag	Hash value of incoming label	Input practical port #	Input virtual port #	Input Label	Output Label	Output virtual port #	Output practical port #
O	$f(\alpha')$	n	A	α''	α''	K	$f(\alpha'')$
O	$f(\beta')$	n	A	β''	β''	K	$f(\beta'')$
O	$f(\gamma')$	n	A	γ''	γ''	X	$f(\gamma'')$
.	$f(\delta')$	2	A	δ''	δ''	B	$f(\delta'')$
O	$f(\varepsilon')$	1	A	ε''	ε''	B	$f(\varepsilon'')$
O	$f(\zeta')$	2	A	ζ''	ζ''	H	$f(\zeta'')$
O	$f(\eta')$	1	A	η''	η''	J	$f(\eta'')$
	$f(\sigma')$	5	A	σ''	σ''	K	$f(\sigma'')$
	$f(\kappa')$	n	A	κ''	κ''	X	$f(\kappa'')$

Figure 11 Fast lookup mechanism using a hash